19-2108; Rev 1; 8/03

EVALUATION KIT AVAILABLE

W-CDMA Upconverter and PA Driver with Power Control

General Description

The MAX2383 upconverter and PA driver IC is designed for emerging ARIB (Japan) and ETSI-UMTS (Europe) W-CDMA applications. The IC includes an upconversion mixer with variable gain control, an LO buffer, and a variable-gain PA driver for output power control.

The MAX2383 is designed to support the IMT-2000 frequency band. It includes a differential IF input port, an LO input port, and PA driver input/output ports. The upconverter mixer incorporates an AGC with over 30dB of gain control. The IC provides automatic throttle-back of PA driver and mixer current as output power is reduced. The main signal path and the LO buffer can be shutdown independently. The on-chip LO buffer can be kept ON while the main transmitter path is being turned on and off to minimize VCO pulling during TX gated-transmission.

The MAX2383 is specified for +2.7V to +3.0V single supply and is housed in an ultra-miniature 3 x 4 UCSP™ package for optimum cost- and space-reduction and for best RF performance. The IC is targeted for the 2270MHz to 2580MHz LO frequency range. It is fabricated using an advanced high-frequency bipolar process. The mixer and PA driver linearity have been optimized to provide excellent RF performance in the 1920MHz to 1980MHz band, while drawing minimal current. The mixer's performance is optimized for a -10dBm ±3dB LO drive at the LO buffer input port. The LO port can be configured to be driven either single-ended or differentially.

The MAX2383 achieves excellent noise and image suppression without the use of an interstage TX SAW bandpass filter, thereby saving valuable board space, cost, and supply current.

For LNA and downconverter mixer companion ICs, see the MAX2387/MAX2388/MAX2389 data sheet.

Applications

Japanese 3G Cellular Phones (ARIB)

European 3G Cellular Phones (UMTS)

Chinese 3G Cellular Phones (TD-SCDMA)

PCS Phones

Pin Configuration appears at end of data sheet.

Typical Operating Circuit appears at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- **+6dBm Output Power with -46dBc ACPR**
- **Ultra-Miniature UCSP Package**
- **Upconverter Gain-Control Range: 35dB**
- **Automatic Dynamic Current Control**
- **12mA Quiescent Supply Current**
- **On-Chip LO Buffer with Disable**
- **Low Out-of-Band Noise Power in RX Band: ≤ -144dBm/Hz at +6dBm P_{OUT}**
- **No Interstage TX SAW Bandpass Filter Required**

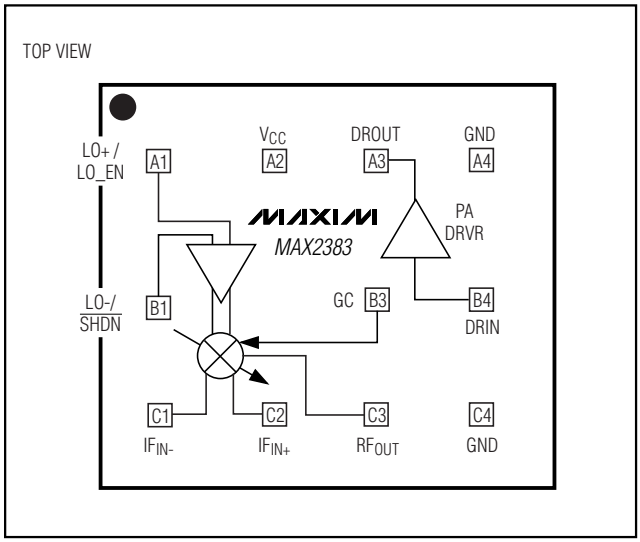
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2383EBC-T	-40°C to +85°C	3 x 4 UCSP

ACTUAL SIZE
UCSP

2mm × 1.5mm

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{CC}, RF_{OUT} to GND .....-0.3V to +6.0V
AC Signals .....+1.0V Peak
$\overline{SHDN}$, LO_EN, V_{GC} to GND .....-0.3V to (V_{CC} + 0.3V)
Digital Input Current ..... ±10mA
Continuous Power Dissipation (T_A = +70°C)
12-Pin UCSP (derate 80mW/°C above +70°C) 628mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (Bump Reflow) .....+235°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.0V, $\overline{SHDN}$ = +1.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +2.85V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7	2.85	3.0	V
Operating Supply Current	I_{CC}	P_{DROUT} = +6dBm, V_{GC} = 2.0V		34	44	mA
		P_{IF} ≤ -35dBm, V_{GC} = 1.4V		12	20	
Shutdown Supply Current	I_{CC}	$\overline{SHDN}$ = 0.5V, LO_EN = 0.5V, V_{GC} = 0.5V		0.5	10	µA
LO Buffer Current	I_{CC}	$\overline{SHDN}$ = 0.5V, LO_EN = 1.5V, V_{GC} = 2V		6	8	mA
Digital Input Logic High	V_{IH}		1.5		V_{CC}	V
Digital Input Logic Low	V_{IL}		0		0.5	V
Input Logic High Current	I_{IH}				1	µA
Input Logic Low Current	I_{IL}		-1			µA
Recommended Gain-Control Voltage	V_{GC}		0.5		2.0	V
Gain-Control Input Bias Current	I_{GC}	0.5V ≤ V_{GC} ≤ 2.0V	-5		5	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2383 EV Kit; V_{CC} = +2.7V to +3.0V; $\overline{SHDN}$ = LO_EN = +1.5V; IF source impedance = 400Ω (differential), IF input level = -16dBm (differential); LO input level = -10dBm, differential LO drive from 150Ω source impedance; mixer upconverter and PA driver are cascaded directly through an interstage matching network; DROUT drives a 50Ω load impedance; V_{GC} = 2.0V; f_{IF} = 380MHz, f_{RF} = 1920MHz to 1980MHz, f_{LO} = 2300MHz to 2360MHz; T_A = -40°C to +85°C. Typical values are at V_{CC} = +2.85V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CASCADED PERFORMANCE (measured from IF input to DROUT (PA driver output))							
IF Frequency	f_{IF}	(Note 2)			200–600		MHz
RF Frequency Range	f_{RF}	(Note 2)		1920		1980	MHz
LO Frequency Range	f_{LO}	High-side LO case (Note 2)			2270–2580		MHz
Output Power (meets ACPR specifications)	P_{DROUT}	V_{GC} = 2.0V	3σ limit	4.4	+6		dBm
			6σ limit	3.8	+6		
Power Gain	G_P	V_{GC} = 2.0V		17	19.5		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2383 EV Kit; V_{CC} = +2.7V to +3.0V; $\overline{SHDN}$ = LO_EN = +1.5V; IF source impedance = 400Ω (differential), IF input level = -16dBm (differential); LO input level = -10dBm, differential LO drive from 150Ω source impedance; mixer upconverter and PA driver are cascaded directly through an interstage matching network; DROUT drives a 50Ω load impedance; V_{GC} = 2.0V; f_{IF} = 380MHz, f_{RF} = 1920MHz to 1980MHz, f_{LO} = 2300MHz to 2360MHz; T_A = -40°C to +85°C. Typical values are at V_{CC} = +2.85V, T_A = +25°C, unless otherwise noted.) (Note 1)

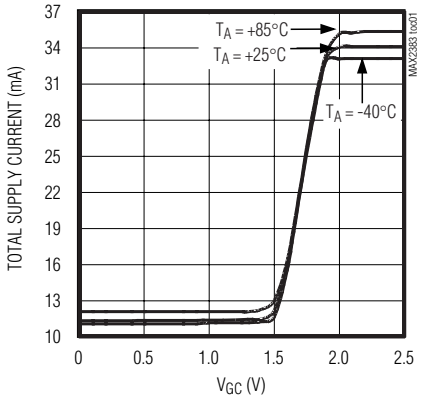
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Control Range		V_{GC} = 0.5V to 2.0V, P_{IF} ≤ -35dBm	25	35		dB
Adjacent Channel Power Ratio	ACPR1	V_{GC} = 2.0V (5MHz offset / 3.84MHz BW)			-46	dBc
Alternate Channel Power Ratio	ACPR2	V_{GC} = 2.0V (10MHz offset / 3.84MHz BW)			-56	dBc
Out-of-Band Noise Power in RX Band		V_{GC} = 2.0V, P_{DROUT} = +6dBm (TX: 1980MHz; RX: 2110MHz)		-144	-140	dBm/Hz
TX In-Band Noise Power		V_{GC} = 2.0V, P_{DROUT} = +6dBm		-139	-135	dBm/Hz
TX In-Band Noise Power		V_{GC} = 0.5V, P_{DROUT} = -35dBm		-147		dBm/Hz
Recommended LO Input Level	P_{LO}	Differential	-13	-10	-7	dBm

Note 1: Minimum and maximum values are guaranteed by design and characterization over temperature and supply voltages.
Note 2: Operation outside this frequency range is possible, but has not been verified.

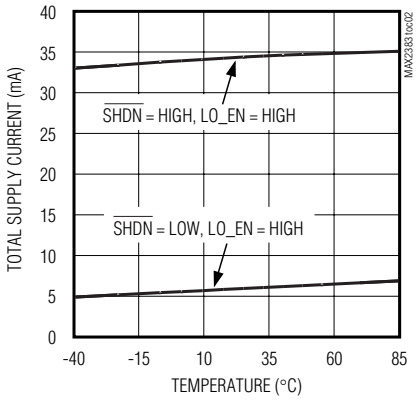
Typical Operating Characteristics

(MAX2383 EV Kit; V_{CC} = +2.85V; $\overline{SHDN}$ = LO_EN = V_{CC}, V_{GC} = 2.0V; IF source impedance = 400Ω (differential), IF input level = -16dBm (differential); LO input level = -10dBm, differential LO drive from 150Ω source impedance; mixer upconverter and PA driver are cascaded through an interstage matching network; DROUT drives a 50Ω load impedance; f_{IF} = 380MHz, f_{RF} = 1950 MHz, f_{LO} = 2330MHz; T_A = +25°C.)

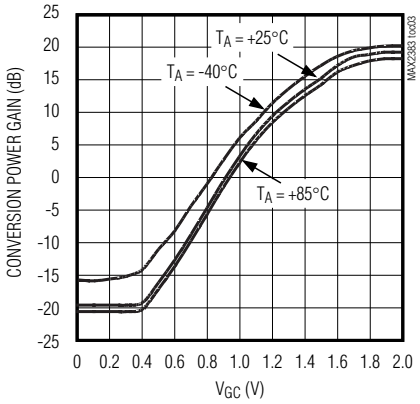
TOTAL SUPPLY CURRENT vs. GAIN-CONTROL VOLTAGE



TOTAL SUPPLY CURRENT vs. TEMPERATURE



CONVERSION POWER GAIN vs. GAIN-CONTROL VOLTAGE



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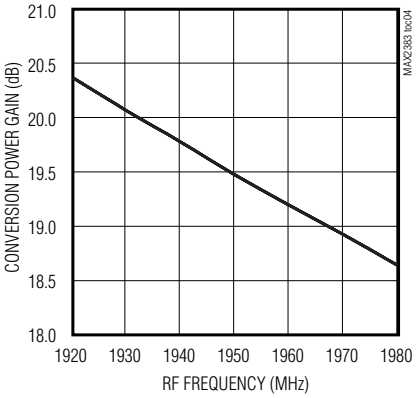
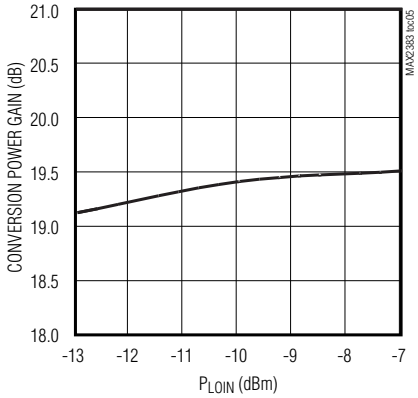
Typical Operating Characteristics (continued)

(MAX2383 EV Kit; V_{CC} = +2.85V; $\overline{SHDN}$ = LO_EN = V_{CC}, V_{GC} = 2.0V; IF source impedance = 400Ω (differential), IF input level = -16dBm (differential); LO input level = -10dBm, differential LO drive from 150Ω source impedance; mixer upconverter and PA driver are cascaded through an interstage matching network; DROUT drives a 50Ω load impedance; f_{IF} = 380MHz, f_{RF} = 1950 MHz, f_{LO} = 2330MHz; T_A = +25°C.)

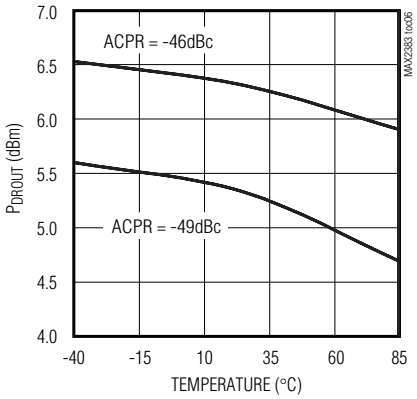
CONVERSION POWER GAIN vs. RF FREQUENCY



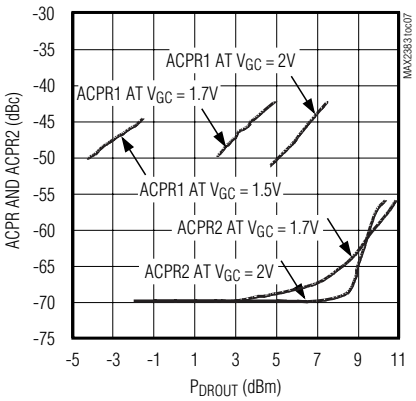
CONVERSION POWER GAIN vs. LO INPUT LEVEL



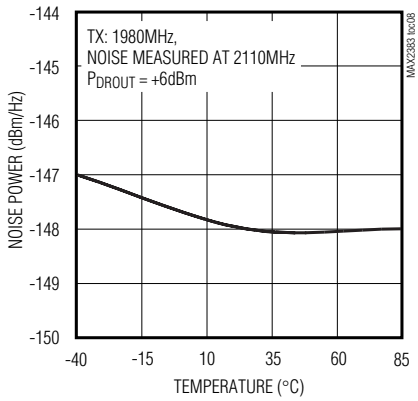
PDROUT vs. TEMPERATURE



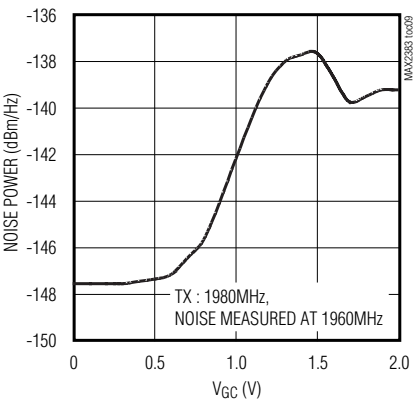
ACPR1 AND ACPR2 vs. PDROUT



RX BAND NOISE POWER vs. TEMPERATURE



INBAND NOISE POWER vs. GAIN-CONTROL VOLTAGE



LO LEAKAGE vs. GAIN-CONTROL VOLTAGE

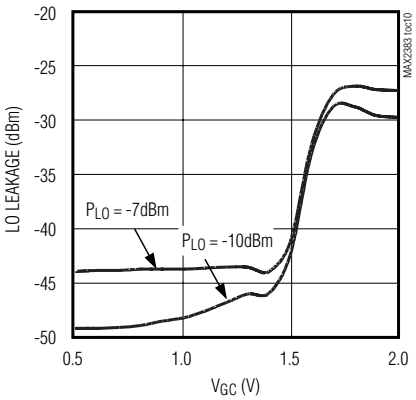
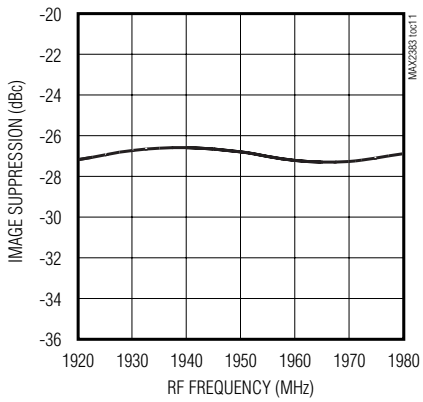
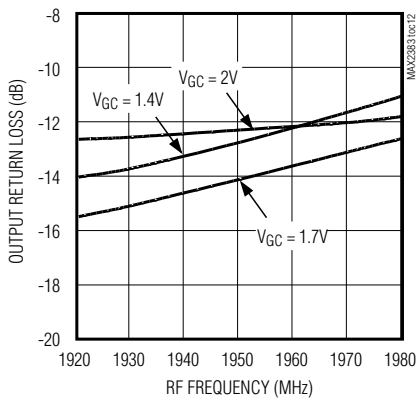


IMAGE SUPPRESSION vs. RF FREQUENCY



OUTPUT RETURN LOSS vs. RF FREQUENCY



Pin Description

PIN	NAME	FUNCTION
A1+	LO_EN /LO+	LO Buffer Enable Pin. When LOW, the LO buffer shuts off. Also noninverting input for LO port. It can be AC-coupled to GND, when the LO is driven single-ended.
A2	V_{CC}	Power-Supply Pin. Bypass with a 330pF capacitor to GND as close to the pin as possible.
A3	DROUT	PA Driver Output Pin. Externally matched to 50Ω.
A4	GND	Ground Reference for RF
B1	$\overline{SHDN}$/ LO-	Shutdown Pin. When LOW, the entire part shuts off, except for LO buffer. Also inverting input for LO port. It can be AC-coupled to GND, when the LO is driven single-ended.
B3	GC	Power Control Input Pin (0.5V to 2.0V for control voltage)
B4	DRIN	PA Driver Input Pin (interstage node). Can be externally matched to 50Ω.
C1	IF_{IN-}	Inverting IF Input (400Ω differential nominal impedance between IF_{IN+} and IF_{IN-})
C2	IF_{IN+}	Noninverting IF Input (400Ω differential nominal impedance between IF_{IN+} and IF_{IN-})
C3	RF_{OUT}	Upconverter Output Port (interstage node). Can be externally matched to 50Ω.
C4	GND	Ground Reference for RF

Detailed Description

Variable-Gain Mixer

The MAX2383 contains a double-balanced Gilbert cell mixer merged with a gain-control circuit, followed by a mixer buffer. The mixer is driven differentially at its IF ports. The LO input for the mixer is conditioned through a low-noise, inductively loaded buffer. The mixer differential output is driven through an on-chip balun into a single-ended common emitter amplifier, which drives the output pin (RF_{OUT}). The mixer buffer is a single-ended in/out common emitter stage with inductive degeneration and an external inductive load. Additionally, these circuits are biased from "VCS" generators, designed to produce a low-noise constant degeneration voltage at the user's current source. These bias circuits also provide the control required to selectively power-down the circuit and also provide for gain control and current throttle-back.

PA Driver

The PA buffer is a single-ended in/out common emitter stage with inductive degeneration and an external inductive load.

Applications Information

LO Buffer Inputs

The external LO is interfaced either differentially or single-ended to the differential LO buffer. Those two pins also function as the control inputs for the device. Hence, they are DC-coupled to the chip-control circuitry, and AC-coupled to the LO port. $\overline{SHDN}$ and LO_EN turn off the whole IC when both pins are pulled LOW. LO_EN helps reduce VCO pulling in gated-transmission mode by providing means to keep the LO buffer on while the upconverter and driver turn on and off. To avoid loading of the LO buffer, connect a 10kΩ isolation resistor between the LO_EN/LO+ pin and the LO_EN logic input, and a 10kΩ isolation resistor between the $\overline{SHDN}$/LO- pin and the $\overline{SHDN}$ logic input.

Differential IF Inputs

The MAX2383 has a differential IF input port for interfacing to differential IF filters. The IF pins should be AC-coupled to the IF ports. The typical IF frequency is 380MHz, but the device can operate from 200MHz to 600MHz. The differential impedance between the two IF inputs is approximately 400Ω in parallel with 1.0pF.

Interstage Matching

The mixer buffer drives the following PA driver through an interstage matching network connected between the mixer's RF_{OUT} pin and the PA driver's input pin (DRIN). This off-chip matching network, which consists of two series inductors and a parallel capacitor, is designed to achieve better than 25dBc image suppression with no current consumption penalty. The quality factor of this off-chip resonant circuit determines the image suppression level and usable bandwidth from the point of view of passband gain flatness.

PA Driver Output

The PA driver output, DROUT, is an open-collector output that requires an external inductor to V_{CC} for proper biasing. The output matching components are chosen

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for optimum linearity and return loss. It is important to tune the interstage matching network components along with the driver output matching components, to achieve the desired cascaded ACPR performance from the whole device.

Layout Issues

For best performance, pay attention to power-supply issues as well as to the layout of the signal lines. The EV kit can be used as a layout example. Ground connections followed by supply bypass are the most important.

Power-Supply and $\overline{SHDN}$ Bypassing

Bypass V_{CC} with a 330pF capacitor to GND as close as possible to the V_{CC} pin. Use separate vias to the ground plane for each of the bypass capacitors and minimize trace length to reduce inductance. Use three separate vias to the ground plane for each ground pin.

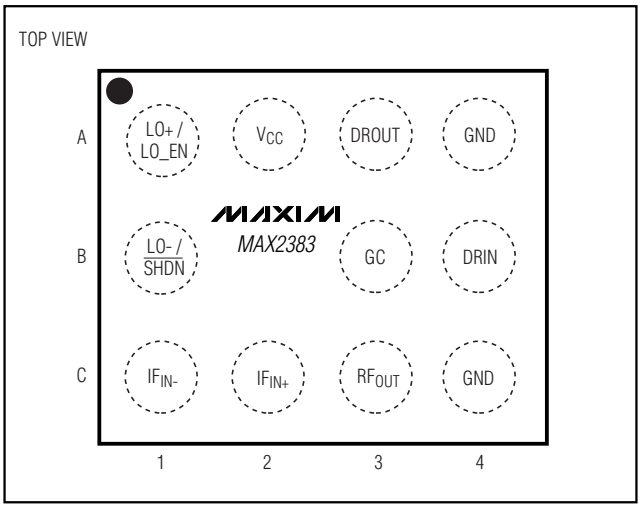
Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration with a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this central node, each going to a separate V_{CC} node in the PC board. At the end of each trace is a bypass capacitor that has low ESR at the RF frequency of operation. This arrangement provides local decoupling at each V_{CC} pin. At high frequencies, any signal leaking out of one supply pin sees a relatively high impedance (formed by the V_{CC} trace inductance) to the central V_{CC} node, and an even higher impedance to any other supply pin, as well as a low impedance to ground through the bypass capacitor.

Impedance-Matching Network Layout

The DROUT and interstage matching networks are very sensitive to layout-related parasitic. To minimize parasitic inductance, keep all traces short and place components as close as possible to the chip. To minimize parasitic capacitance, minimize the area of the plane.

Pin Configuration



UCSP Reliability

The chip-scale package (UCSP) represents a unique package that greatly reduces board space compared to other packages. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP. This form factor may not perform equally to a packaged product through traditional mechanical reliability tests. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a UCSP. UCSP solder joint contact integrity must be considered since the package is attached through direct solder contact to the user's PC board. Testing done to characterize the UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website, www.maxim-ic.com.

Chip Information

TRANSISTOR COUNT: 998

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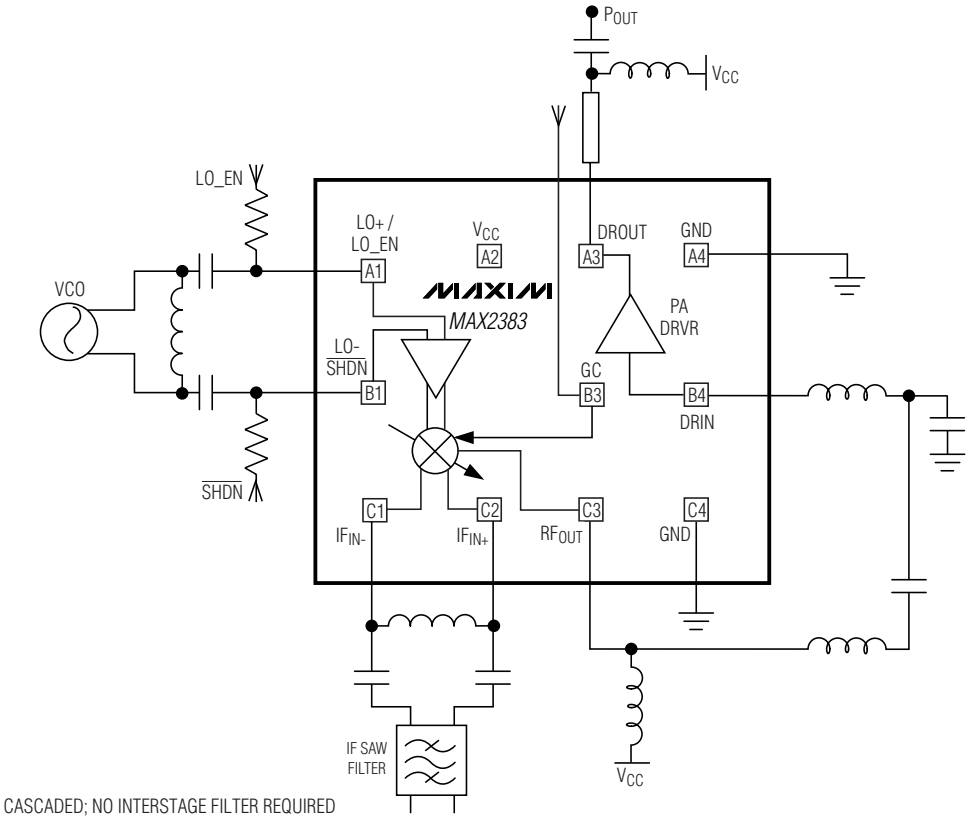
Typical Operating Circuit



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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)